A HIGH SPEED, STATIC DIGITAL MULTIPLEXER

ABSTRACT OF THE DISCLOSURE

A high speed static multiplexer comprising: (1) a plurality of data inputs and at least one select input; (2) an output; (3) a high voltage rail and a low voltage rail; (4) a pull-up circuit coupled between the output and the high voltage rail and further coupled to receive the data inputs and the select input so that the pull-up circuit generates a first logic state at the output in response to the selected data input having that first logic state; (5) and a pull-down circuit coupled between the output and the low voltage rail and further coupled to receive the data inputs and the select input, so that the pull-down circuit generates a second logic state at the output in response to the selected data input having that second logic state.